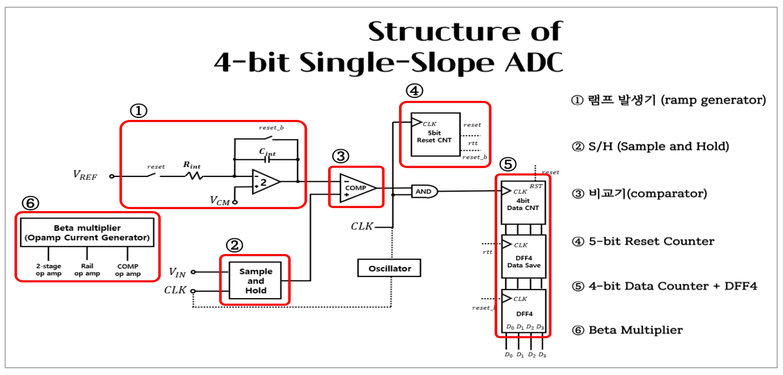
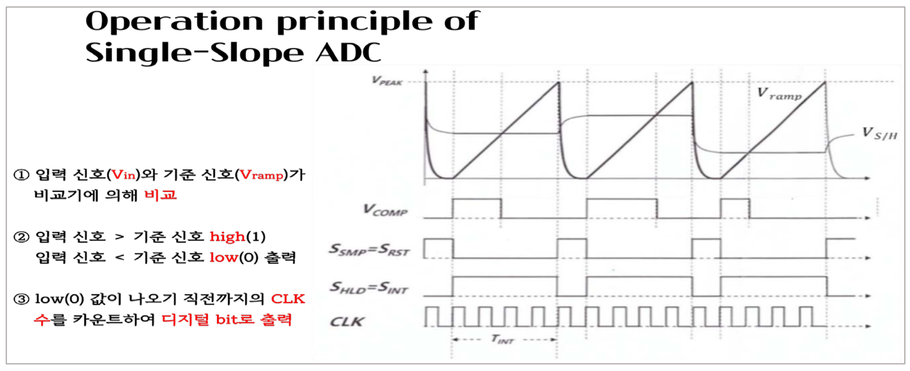
IDEC Chip Design Contest

4-bit Single Slope ADC for Temperature Sensor

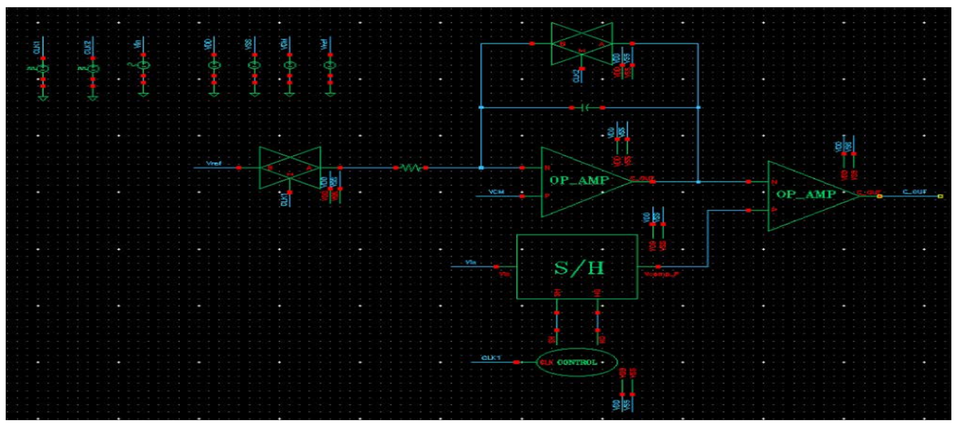
Back Lee[1], Yun-Ju Park[1], Sung-Il Choi[1], Jae-Eun Jang[1], Seong-Ik Cho[2]
Jeonbuk National University

Analog to Digital Converter is a device that converts various analog signals into digital values. ADCs are essential for computers to process digital signals. Single-Slope ADC (SS-ADC) is an ADC with higher accuracy than other ADC types, so it is widely used for sensors that require accurate and multiple arrays. The operating principle of the proposed SS-ADC is as follows When an input signal enters the SS-ADC, the value entering the comparator is fixed through S/H. The input signal after the S/H operation and the reference voltage signal generated through the ramp generator are transferred to one comparator, and the two signals output high (1) if the input signal is greater than the ramp signal, and low (0) if it is smaller. print out. The counter transmits clock pulses to the D flip-flop until the ramp signal matches the input signal, that is, just before a value of 0 is output to the comparator. The number of clocks received from D F/F is displayed as a 4-bit digital output, and after all operations, a 5-bit reset counter generates signals used by switches and counters to reset the SS-ADC to its initial state. The proposed SS-ADC simplifies the control logic and improves accuracy by synchronizing with clk. Through this, the analog temperature voltage is converted into a digital 4-bit code and is designed to be divided into 16 steps using a temperature sensor that outputs an analog signal of 0.5V at 0°C and 1.5V at 100°C.

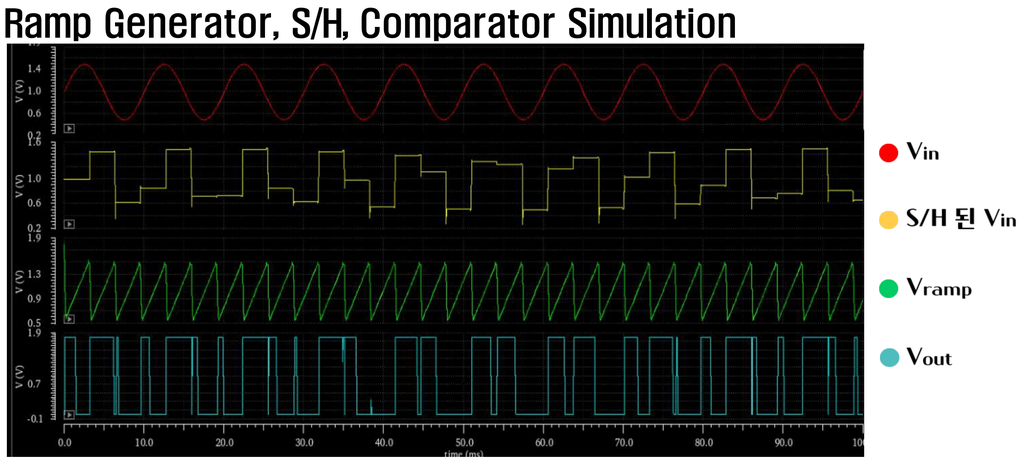




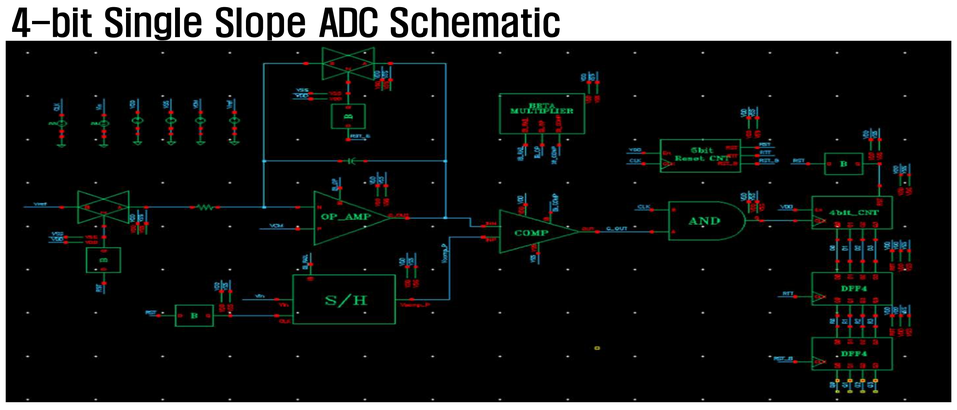
Ramp Generator, S/H, Comparator



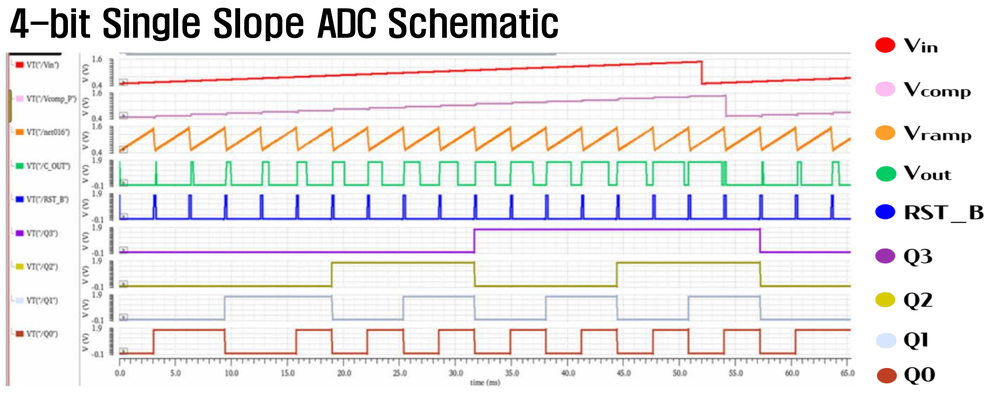
Ramp Generator, S/H, Comparator Simulation



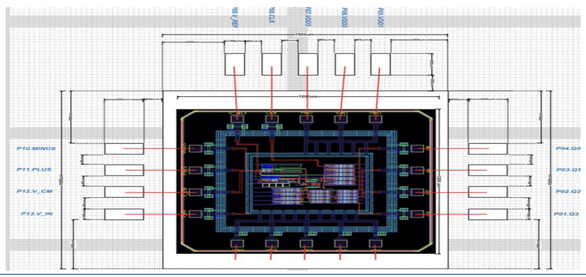
4-bit Single Slope ADC Schematic

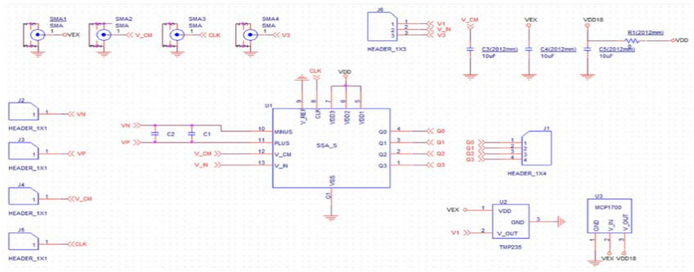


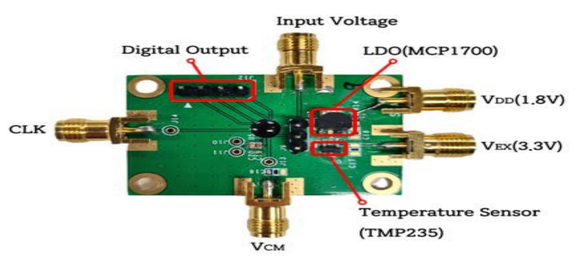
4-bit Single Slope ADC Schematic



Layout 및 CoB

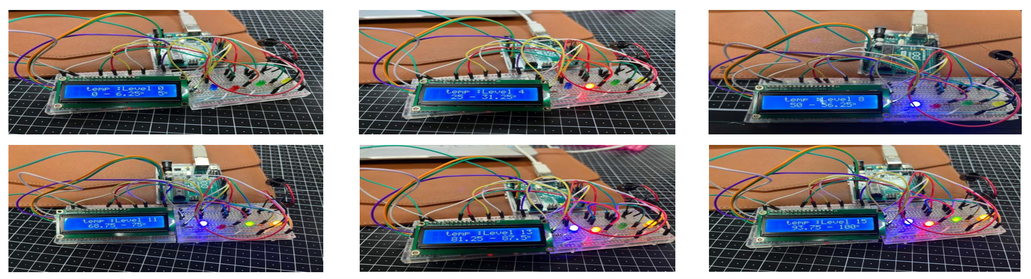






칩 시연

온도 범위 (°C)	전압 범위 (V)	Digital 4-bit	LED (BRGY)	CLCD	Piezo (소리)
0 ~ 6.25	0.5 ~ 0.5625	0000	– – – –	Level 0	X
6.25 ~ 12.5	0.5625 ~ 0.625	0001	– – – Y	Level 1	X
12.5 ~ 18.75	0.625 ~ 0.6875	0010	– – G –	Level 2	X
18.75 ~ 25	0.6875 ~ 0.75	0011	– – G Y	Level 3	X
25 ~ 31.25	0.75 ~ 0.8125	0100	– R – –	Level 4	X
31.25 ~ 37.5	0.8125 ~ 0.875	0101	– R – Y	Level 5	X
37.5 ~ 43.75	0.875 ~ 0.9375	0110	– R G –	Level 6	O
43.75 ~ 50	0.9375 ~ 1	0111	– R G Y	Level 7	O
50 ~ 56.25	1 ~ 1.0625	1000	B – – –	Level 8	O
56.25 ~ 62.5	1.0625 ~ 1.125	1001	B – – Y	Level 9	O
62.5 ~ 68.75	1.125 ~ 1.1875	1010	B – G –	Level 10	O
68.75 ~ 75	1.1875 ~ 1.25	1011	B – G Y	Level 11	O
75 ~ 81.25	1.25 ~ 1.3125	1100	B R – –	Level 12	O
81.25 ~ 87.5	1.3125 ~ 1.375	1101	B R – Y	Level 13	O
87.5 ~ 93.75	1.375 ~ 1.4375	1110	B R G –	Level 14	O
93.75 ~ 100	1.4375 ~ 1.5	1111	B R G Y	Level 15	O



A 4-bit SS-ADC that requires accuracy was designed using the DB Hitech 180nm process. The DC gain of the ramp generator 2-stage opamp is 79.65 PM at 84.5°, the S/H rail-to-rail opamp DC gain is 118.22 PM at 80.9°, and the comparator DC gain is 198.7. The capacitor of the lamp generator can be connected externally, a 5-bit reset counter is used as the switch control logic, and a 4-bit SS-ADC specialized for the temperature sensor is used to provide a voltage between 0 and 100 degrees within a 1.8V supply voltage of 0.5V to 1.5V. V has an input voltage. Lamp generator, S/H circuit, and comparator are designed as amplifiers suitable for each characteristic to reduce MOS usage and minimize power and layout area. The S/H switch adjusts the slip rate to prevent switch timing errors. The digital block is designed to be synchronized with the falling edge to avoid gate delay.
If the resolution is increased, the operation speed is slowed down, so a method to solve this problem will be studied and needed. If this problem is improved in the 4th industrial revolution, SS-ADC is expected to be used in various systems that require temperature stability.

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.